CLAIMS

What is claimed is:

1. A method for customization of a FPGA-based SoC, the method comprising:

selecting a system component used for customizing the FPGA-based SoC;

configuring said selected system component with parameters for use with the FPGA-based SoC;

propagating said parameters used to configure said selected system component to peer system components; and

configuring said peer system components using said propagated parameters during customization of the FPGA-based SoC.

2. The method according to claim 1, further comprising configuring the selected system component with parameters used to configure said peer system component.

3. The method according to claim 2, further comprising the step of propagating said parameter used to configure said peer system component to subsequently selected system components used to configure the FPGA-based SoC.

4. The method according to claim 1, wherein said selecting step further comprises the step of providing an option for selecting an implementation selected from the group consisting of a hardware implementation and a software implementation.

5. The method according to claim 1, wherein said step of selecting said system component further comprises selecting a system component from the group consisting of a hardware core

and a software core.

6. The method according to claim 1, wherein the method further comprises the step of initializing only the selected system components that are utilized for customizing the FPGA-based SoC.

7. A machine readable storage having stored thereon, a computer program having a plurality of code sections, said code sections executable by a machine for causing the machine to perform the steps of:

selecting a system component used for customizing a FPGA-based SoC;

configuring said selected system component with parameters for use with said FPGA-based SoC;

propagating said parameters used to configure said selected system component to peer system components; and

configuring said peer system components using said propagated parameters during customization of said FPGA-based SoC.

8. The machine readable storage according to claim 7, further comprising sections of code for causing the machine to configure the selected system component with parameters used to configure said peer system component.

9. The machine readable storage according to claim 8, further comprising sections of code for causing the machine to propagate said parameter used to configure said peer system component to subsequently selected system components used to configure said FPGA-based SoC.

10. An interface for integrating hardware system component cores used for customizing a FPGA-based SoC, the interface

comprising:

a slave connection circuitry communicatively interfaced to a processor bus;

a master connection circuitry communicatively interfaced to said processor bus; and

a multiplexer for selecting one of said slave connection circuitry and said master connection circuitry for providing communication between a processor bus and a selected hardware system component core used for customizing the FPGA-based SoC.

11. The interface for integrating hardware system component cores according to claim 10, wherein said selected hardware system component core is a proprietary customer specific hardware core.

12. The interface for integrating hardware system component cores according to claim 10, wherein said selected hardware system component core is a commercially available hardware core.

13. The interface for integrating hardware system component cores according to claim 10, further comprising a direct memory access (DMA) controller for providing direct access to a memory device.

14. The interface for integrating hardware system component cores according to claim 13, further comprising a write buffer and a read buffer, said write buffer and said read buffer providing temporary storage of I/O data from said memory device for said selected hardware system component core.

15. The interface for integrating hardware system component cores according to claim 10, further comprising an interrupt controller coupled to said multiplexer, said interrupt controller for latching individual interrupt signals and providing a signal to a microprocessor indicating an interrupt condition.

16. A GUI for integrating system component cores during customization of a FPGA-based SoC, the GUI comprising:

a selection object for providing selection of a system component core for customizing the FPGA-based SoC;

a configuration object for configuring said selected system component core and peer system component; and

a display object for displaying parameters used by said configuration object to configure said selected system component core and peer system components.

17. The GUI according to claim 16, wherein said configuration object further comprises a parameter distribution object for distributing said parameters to subsequently selected system component cores and peer system components.

18. The GUI according to claim 16, wherein said selection object further comprises a dialog for selecting hardware system component cores and software system component cores.